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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/325,099	06/03/1999	ALEXANDER SHVARTS	4498	2396

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EXAMINER	
KIM, KEVIN	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 12/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

SP

Office Action Summary	Application No.	Applicant(s)	
	09/325,099	SHVARTS ET AL.	
	Examiner	Art Unit	
	Kevin Y. Kim	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,7-12,14 and 16-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,7-12,14 and 16-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9-29-2006 has been entered.

Response to Arguments

2. Applicant's arguments filed September 29, 2006 have been fully considered but they are not persuasive.

Examiner highly appreciates applicant's effort to provide an answer to the question of how to provide the switching functionality for a dual band system. The Declaration of Mr. Jonathan Strange is fully considered and it is persuasive in that PIN diodes, MESFET transistors or a cascade current switch had been well known prior to the filing date of the present invention. The statement that "The connection paths would be hardwired, and the appropriate signal would be chosen by applying a switching voltage or current" is also accepted as explaining how the switches operate. But this Declaration fails to show the alternative relationships $F_{LO} = F_{OUT} / (1 + m/n)$ and $F_{LO} = F_{OUT} / (1 - m/n)$ would occur as a result of the switching operation.

Applicant quotes page 9, lines 7-9 as supporting material for enablement of the dual mode switching such as defined in claim 1. In order for the quotation to meet the disclosure requirement under 35 USC 112 first paragraph, one should be able to see that, when the switch

100 couples the output of VCO 90 to the downconverter mixer 80, one of the relationships, i.e., $F_{LO} = F_{OUT} / (1 + m/n)$ should occur, and when the switch 100 couples the output of VCO 92 to the downconverter mixer 80, the other of the relationships, i.e., $F_{LO} = F_{OUT} / (1 - m/n)$ should occur. However, despite a careful study of Fig.3 and its description, this examiner has not been able to find that is the case. For one, the specification fails to distinguish VCO 90 from VCO 92. See page 9, lines 2-3. If these are no different from each other, the result would be the same regardless of which is connected to the mixer 80.

And yet, the description at page 9, lines 3-6 stating that "[t]he transmitter output may be switched between each output path to provide operation at [sic] of two transmission standards" somewhat supports that the switching could be what enables the switching between $F_{LO} = F_{OUT} / (1 + m/n)$ and $F_{LO} = F_{OUT} / (1 - m/n)$ recited in the claim, as best understood by exmaminer.

In order to advance the prosecution of the present invention, the derivation of the recited alternative relations between F_{LO} and F_{OUT} in accordance with the switching between VCO 90 and VCO 92 is highly suggested to examiner's satisfaction. Until such a showing is provided, the rejection of the claims as provided for in the last Office action is sustained.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

4. Claims 1, 5, 7-10, 14,16-19, 21 and 22 are rejected under 35 U.S.C. 102(a) as being anticipated by Herzinger (EP 0 905 879 A1, previously cited).

Claim 1.

Herzinger discloses a translation loop modulator (see Fig. 2 and the English abstract) for transmission circuit in a communication system, said translation loop modulator comprising: 1) input modulation means ("QM" and "BP") for receiving at least one input signal ("f_I" and "f_Q") that is representative of information to be modulated, for receiving a feedback signal (f_{MO}), and for producing an intermediate modulated signal (output from "BP" responsive to said input signal and said feedback signal);

2) comparator means ("FT1" "FT2" "PFD" "CP" "LF" and "HF-VCO") for receiving said intermediate modulated signal (output from "BP") and a reference signal ("f_{LO}") having a frequency of F_{LO}, and for producing an output transmission signal ("A" having a frequency of f_{VCO} responsive to said intermediate modulated signal and said reference signal, wherein said comparator means includes a first frequency divider unit ("FT1") for providing a divide by m function and a second frequency divider unit ("FT2") for providing a divide by n function such that $f_{LO} = f_{VCO} / (1 - m/n)$ (see the mathematical expression in col. 4, line 49, also see right column on page 3 of the English translation of DE 19743207 provided by the applicant), and

3) feedback circuitry ("M1" and "TP") coupled to said output transmission signal ("A"), coupled to said reference signal ("f_{LO}") and coupled to said input modulation means ("QM" and "BP"), said feedback circuitry for producing said feedback signal ("f_{MO}") responsive to said output transmission signal and said reference signal.

The claim appears to be different in that it further describes that the two frequency divider are provided such that the translation loop module operates in a second mode where $F_{LO} = F_{OUT} / (1 + m/n)$. However, up on a closer look, the claimed invention recites no mechanism to switch between two modes. It merely defines that, presumably by a selection element (but not

recited), the module could operate in either mode. In that sense, the translation loop module, having all the claimed elements of the claimed invention, is equally capable of operating in the two modes, where in the second mode the difference f_{VCO}-f_{LO} is taken instead of f_{LO}-f_{VCO}, resulting in $F_{LO} = F_{OUT} / (1 - m/n)$.

In other words, all the elements of the claimed invention are found in the Herzinger reference.

Claim 5.

Herzinger also teaches an input port of said second frequency divider unit ("FT2") is coupled to said reference signal (f_{LO} output from "LO"), and an output port of said second frequency divider unit is coupled to a phase comparator device (PFD).

Claim 7.

Herzinger also teaches an input port of said first frequency divider unit ("FT1") is coupled to said intermediate modulated signal (the output from "BP" in Fig. 2), and said output port of said first frequency divider unit is coupled to a phase comparator device ("PFD").

Claim 8.

Herzinger also teaches said feedback circuitry ("M1" and "TP") includes a mixer device ("M1") including a first input port coupled to said output transmission signal ("A"), a second input port coupled to said reference signal ("f_{LO}"), and an output port coupled to said feedback signal ("f_{MO}").

Claim 9.

Herzinger also teaches said reference signal is directly connected to said mixer device (as seen in Fig. 2, the reference signal "f_{LO}" is directly connected to the mixer device "M1").

Claim 10.

Herzinger discloses a translation loop modulator (see Fig. 2 and the English abstract) for transmission circuit in a communication system, said translation loop modulator comprising:

1) input modulation means ("QM" and "BP") for receiving at least one input signal ("f_I" and "f_Q") that is representative of information to be modulated, for receiving a feedback signal (f_{MO}), and for producing an intermediate modulated signal (output from "BP" responsive to said input signal and said feedback signal);

2) comparator means ("FT1" "FT2" "PFD" "CP" "LF" and "HF-VCO") for receiving said intermediate modulated signal (output from "BP") and a reference signal ("f_{LO}") having a frequency of F_{LO}, and for producing a phase comparator signal responsive to said intermediate modulated signal and said reference signal, wherein said comparator means includes a first frequency divider unit ("FT1") for providing a divide by m function and a second frequency divider unit ("FT2") for providing a divide by n function;

3) oscillation means("HF-VCO") for receiving said phase comparator signal (output from "LF") and for producing an output transmission signal ("A" in Fig. 2) responsive to said phase comparator signal, said output transmission signal having a frequency such that $f_{LO} = f_{VCO} / (1 -$

m/n) (see the mathematical expression in col. 4, line 49, also see right column on page 3 of the English translation of DE 19743207 provided by the applicant), and

4) feedback circuitry ("M1" and "TP") coupled to said output transmission signal ("A"), coupled to said reference signal ("f_{LO}") and coupled to said input modulation means ("QM" and "BP"), said feedback circuitry for producing said feedback signal ("f_{MO}") responsive to said output transmission signal and said reference signal.

The claim appears to be different in that it further describes that the two frequency divider are provided such that the translation loop module operates in a second mode where $F_{LO} = F_{OUT} / (1 + m/n)$. However, up on a closer look, the claimed invention recites no mechanism to switch between two modes. It merely defines that, presumably by a selection element (but not recited), the module could operate in either mode. In that sense, the translation loop module, having all the claimed elements of the claimed invention, is equally capable of operating in the two modes, where in the second mode the difference f_{VCO}-f_{LO} is taken instead of f_{LO}-f_{VCO}, resulting in $F_{LO} = F_{OUT} / (1 - m/n)$.

In other words, all the elements of the claimed invention are found in the Herzinger reference.

Claim 14.

Herzinger also teaches an input port of said second frequency divider unit ("FT2") is coupled to said reference signal (f_{LO} output from "'LO"), and an output port of said second frequency divider unit is coupled to a phase comparator device ("PFD").

Claim 16.

Herzinger also teaches an input port of said first frequency divider unit ("FT1") is coupled to said intermediate modulated signal (the output from "BP"), and an output port of said first frequency divider unit is coupled to a phase comparator device ("PFD").

Claim 17.

Herzinger also teaches said feedback circuitry (M1 and TP) includes a mixer device ("M1" in Fig. 2) including a first input port coupled to said output transmission signal ("A" in Fig. 2), a second input port coupled to said reference signal (" f_{LO} "), and an output port coupled to said feedback signal ("f_{MO}" in Fig. 2).

Claim 18.

Herzinger also teaches said reference signal is directly connected to said mixer device (as seen in Fig. 2, the reference signal " f_{LO} " is directly connected to the mixer device M1.

Claim 19.

Herzinger teaches a translation loop modulator (seeFig. 2 and the English abstract) for a transmission circuit in a communication system, said translation loop modulator comprising:

quadrature modulation means (QM and BP in Fig. 2) for receiving at least one input signal ("f_I" and "f_Q") that is representative of information to be modulated, for receiving a feedback signal (f_{MO}) , and for producing a quadrature modulated signal (output from "BP" in Fig. 2) responsive to said input signal and said feedback signal,

first frequency divider means (FT1) for receiving said quadrature modulated signal (output from BP), and for producing a first frequency divided signal (output from "FTI") responsive to said quadrature modulated signal such that said first frequency divider means provides a divide by m function,

second frequency divider means (FT2) for receiving a reference signal (f_{LO}), and for producing a second frequency divided signal (f_{PD}) responsive to said reference signal such that said first frequency divider means provides a divide by n function,

phase comparator means ("PFD" "CP" and "LF" in Fig. 2) for re reiving said first frequency divided signal and said second frequency divided signal, and for producing a phase comparator signal (output from LF) responsive to said first and second frequency divided signals;

oscillator means (HF-VCO) for receiving said phase comparator signal (output from "LF" in Fig. 2), and for producing an output transmission signal ("A" in Fig. 2) having a frequency F_{OUT} responsive to said phase comparator signal such that $f_{VCO} = f_{LO} (1 - m/n)$ (see the mathematical expression in col. 4, line 49; also see right column on page 3 of the English translation of DE 19743207 provided by the applicant); and

feedback circuitry ("M1" and "TP" in Fig. 2) coupled to said output transmission signal (A), coupled to said reference signal (f_{LO}) and coupled to said quadrature modulation means ("QM" and "BP" in Fig. 2), said feedback circuitry for producing said feedback signal (f_{MO}) responsive to said output transmission signal and said reference signal.

The claim appears to be different in that it further describes that the two frequency divider are provided such that the translation loop module operates in a second mode where F_{LO}

$= F_{OUT} / (1 + m/n)$. However, up on a closer look, the claimed invention recites no mechanism to switch between two modes. It merely defines that, presumably by a selection element (but not recited), the module could operate in either mode. In that sense, the translation loop module, having all the claimed elements of the claimed invention, is equally capable of operating in the two modes, where in the second mode the difference f_{VCO}-f_{LO} is taken instead of f_{LO}-f_{VCO}, resulting in $F_{LO} = F_{OUT} / (1 - m/n)$.

In other words, all the elements of the claimed invention are found in the Herzinger reference.

Claim 22.

Herzinger discloses operating the translation loop module in GSM mode (about 900 MHz).

Claim Rejections - 35 USC § 103

5. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Herzinger, as applied to claim 19 above, in view of Damgaard et al. (U.S. Patent No. 6,208,875, cited previously).

Herzinger discloses all the subject matter claimed except for operating at about 1800 MHz. Damgaard et al teaches dual mode translation loop module which can operate at about 1800 MHz as well as at about 900 Mhz. Thus, it would have been obvious to one skilled in the art at the time the invention to select parameters of Herzinger's module such that it can operate at about 1800 MHz to provide communication capability for the DCS mode.

6. Claim 2, 3, 11, 12 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herzinger, as applied to claims 1,10 and 19 above, in view of Jaffe (US Patent 5,130,670).

Claims 2,11 and 20.

Herzinger teaches the claimed including an oscillating means ("LO") for generating the reference signal ("f_{LO}"), but fails to teach that the oscillating means is a reference loop modulator, i.e., a feedback loop configuration. Jaffe teaches that an oscillating means (16 in Fig. 4) is implemented with a phase locked loop (52', 54', 56', 58' 66, 64' 60' and 62' in Fig. 7). The phase locked loop comprises a stability enhancement circuit (66 in Fig. 7) so as to generate a stable output oscillating signal. It is desirable to generate a stable reference signal in the translation loop modulator of Herzinger so as to generate a stable output transmission signal (A).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the oscillating means of Herzinger with a phase locked loop, as taught by Jaffe, so as to generate a stable reference signal and consequently to generate a stable output transmission signal.

Claims 3 and 12.

Jaffe teaches the claimed limitation "said reference loop modulator includes a fractional n synthesizer" because Jaffe teaches that the oscillating means 16 is a fractional n synthesizer (col. 16, lines 62-63).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Y. Kim whose telephone number is 571-272-3039. The examiner can normally be reached on 8AM --5PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

December 4, 2006

AU 2611

/Kevin Kim/

KEVIN KIM
PRIMARY PATENT EXAMINER